FIG. 1

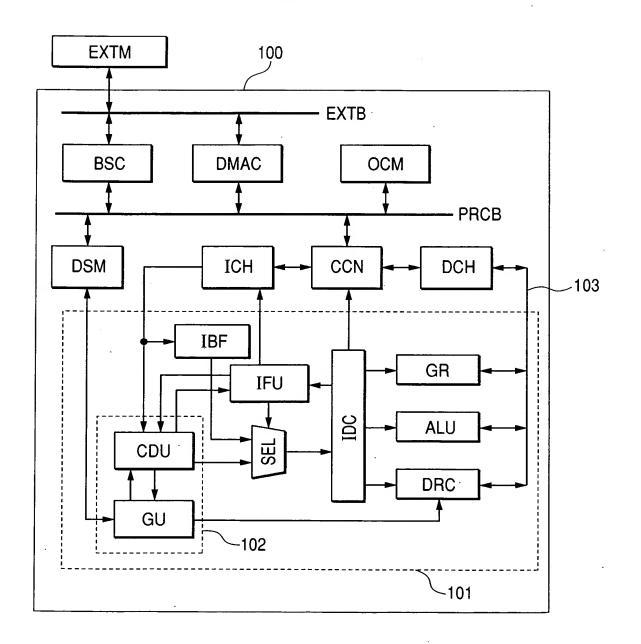


FIG. 2

LOOP FREQUENCY	OPERATION OF DRC CONTROL UNIT 102	SOFTWARE TO BE EXECUTED
FIRST TIME	TEMPORARY DECISION	NORMAL SW
SECOND TIME	NORMAL SW ACQUISITION FINAL DECISION	NORMAL SW
THIRD TIME	DRC RECONFIGURATION	NORMAL SW
FOURTH TIME		DRC DRIVER SW
FIFTH-n-TH TIME		DRC DRIVER SW

FIG. 3

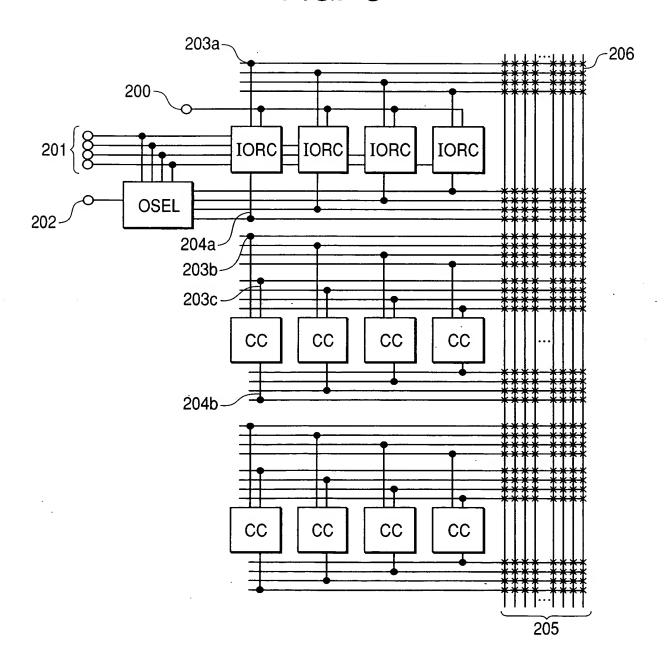


FIG. 4

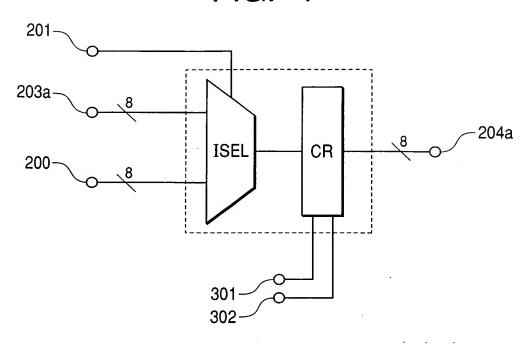


FIG. 5

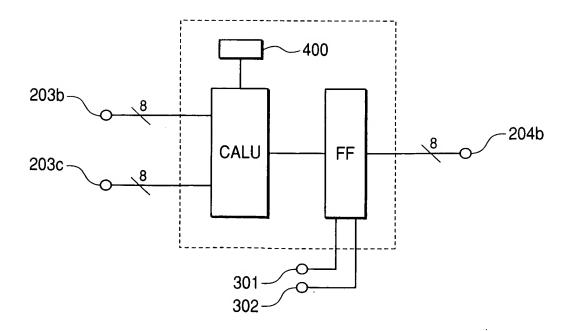
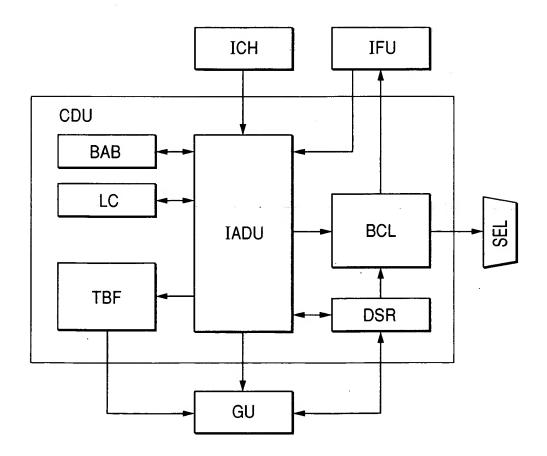
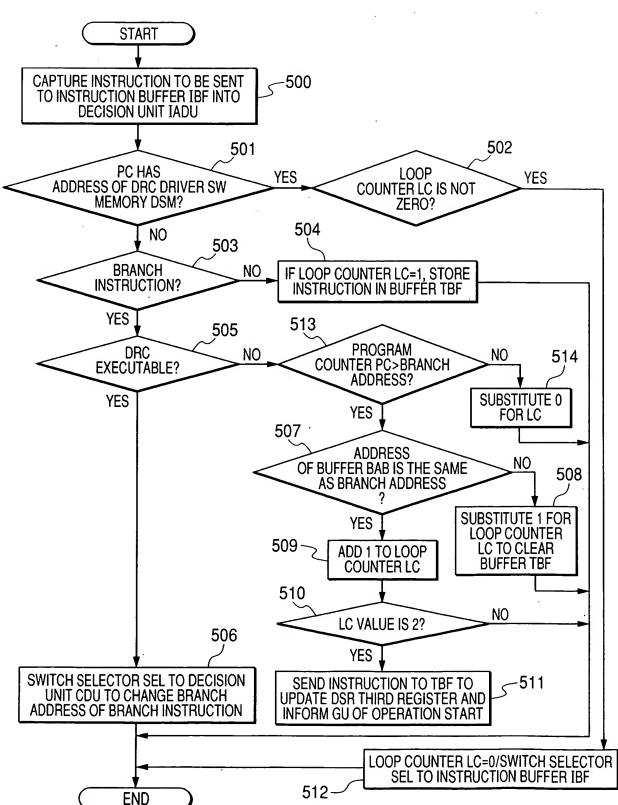


FIG. 6







## FIG. 8

*(A)* 

**(B)** 

_	•	
1 2 3 4 5 6 7 8 9 10 11 12	L002: DT MOV MOV MUL MOV STS SUB MOV MOV ADD	R0 @R6,R3 @R5,R2 R3,R2 @R4,R1 MACL,R7 R7,R1 R1,@R5 @R4,R3 R3,R7 R7,@R4
		•
13 14	ADD ADD	#4,R4 #4,R5
15	BF	L002

(C)

	T	<del></del>
1	MOV	R6,dR6
2	MOV	R5,dR5
2 3 4	MOV	R4,dR4
4	L002a:	
5	MOV	@dR6,dR3
6 7	MOV	@dR5,dR2
7	MOV	@dR4,dR1
8	DT	R0
9	MOV	dR1,@dR5
10	MOV	dR7,@dR4
11	NOP	
12	BF	L002a
13	MOV	dR5,R5
14	MOV	dR4,R4
15	JMP	L003

(D)

DATA TRANSFER INSTRUCTION
ADDITION INSTRUCTION
SUBTRACTION INSTRUCTION
MULTIPLICATION INSTRUCTION
DECREMENT+BRANCH SET INSTRUCTION
BRANCH INSTRUCTION
NONBRANCH INSTRUCTION
NO OPERATION
SYSTEM REGISTER LOAD
SYSTEM REGISTER STORE
RETURN INSTRUCTION
GENERAL REGISTER*
IORC*

FIG. 9

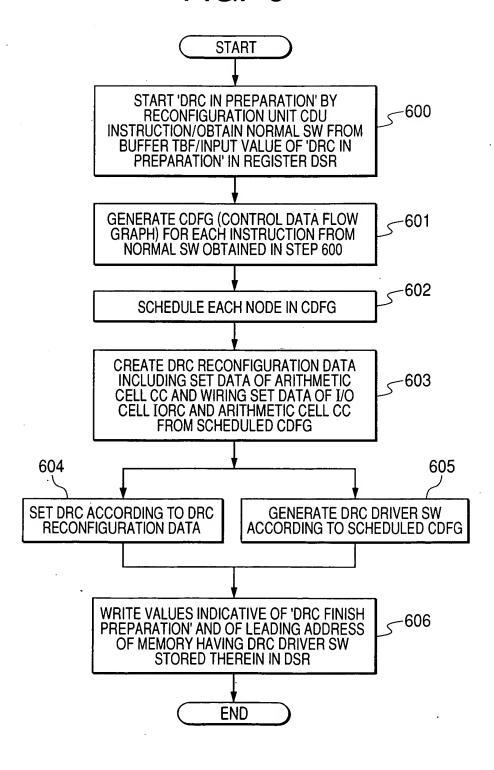
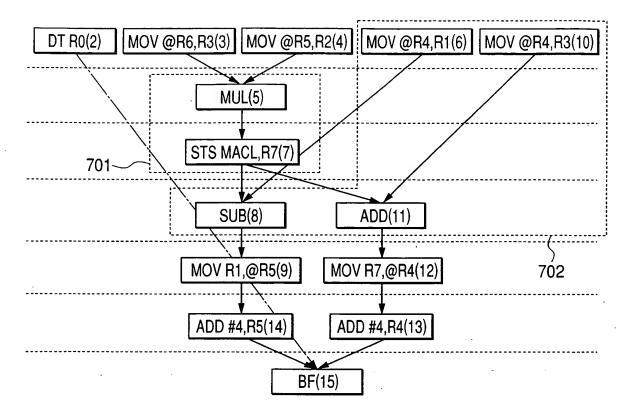
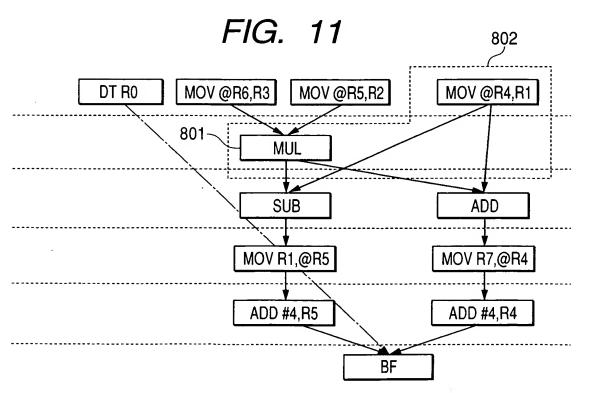


FIG. 10





10 / 12

FIG. 12

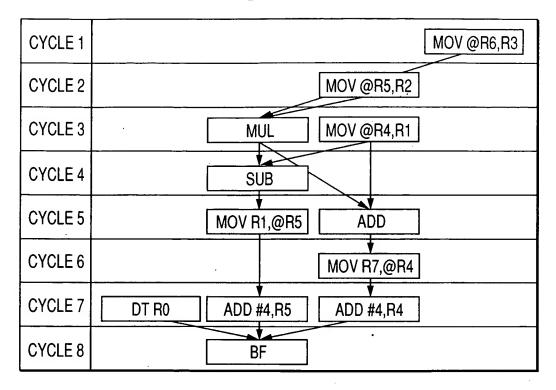


FIG. 13

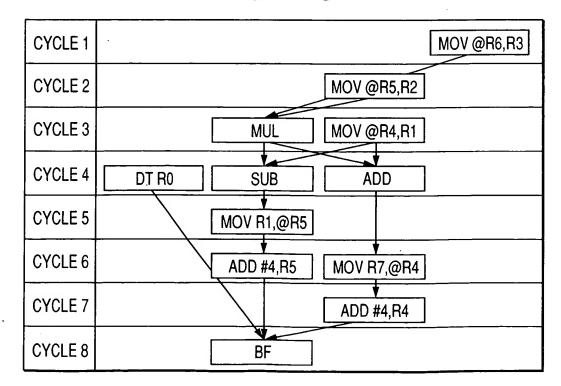


FIG. 14

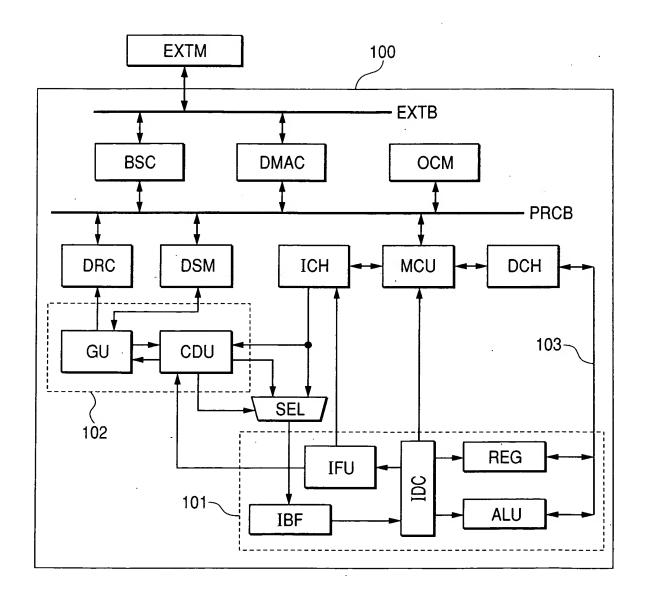


FIG. 15

